DRAFT AMENDMENT

U. S. Patent Application of NITTA et al.
Application No.: 09/739,737; Filed: December 20, 2000
For: DISPLAY APPARATUS
Your Reference No.: P00-10-1US
Our Reference No.: SUT-0004 *(formerly 107254-00004)*
Our File No. 85254-0004

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Amended) A display apparatus for displaying images based on signals received from a host, comprising:

determining means for determining ~~an interface type of~~ an appropriate one of a plurality of interface types to connect the display apparatus and said host;

a plurality of storage means each storing specification information relating to the display for each one of the interface types to be connected; and

output means for switching between or among the plurality of storage means based upon the determination by the determining means and for outputting, from said storage means to said host, the specification information corresponding to the appropriate one of the interface ~~type~~ types determined by said determining means.

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Goddard et al. merely discloses two types of interfaces, a graphics processor and a VGA sub-system, each of which is connected to memories through an exclusive line and the like. That is, this construction does not send to the host the specification information corresponding to an interface type. This reference neither discloses nor suggests the characterizing feature of the present invention at all.

In the first place, Goddard et al. and the present invention are different in what is stored in the storage means.

That is, what is stored in the storage means of the present invention is the specification information corresponding to the interface type, i.e. EDID. It is image data that is stored in "COMBINED MEMORY IMAGES 3" and "VGA IMAGE PLUS REGISTERS 8" of Goddard et al. which correspond to the storage means of the present invention. This is clear from the statement in Goddard et al., Col. 4, lines 5-13, "Merging means 1 a are provided between ... into some location of the high level memory part 3."

Furthermore, the storage means of Goddard et al. have inputs each connected to a different signal source. "GRAPHIC PROCESSOR 1" is connected to "COMBINED MEMORY IMAGE 3", and "VGA HARDWARE SUB-SYSTEM7" to "VGA IMAGE PLUS REGISTER 8". An external output is provided only for "COMBINED MEMORY IMAGES 3". Output of "VGA IMAGE PLUS REGISTER 8" is connected to "COMBINED MEMORY IMAGES 3" through "BLOCK COPY 1a". Each storage means plays the role of a buffer.

On the other hand, "EDID storage memory 23" and "EDID storage memory 25" which are the storage means of the present invention have only outputs, and not inputs. This is because EDID is storied beforehand, and there is no need for receiving input from outside. The outputs of "EDID storage memory 23" and "EDID storage memory 25" are connected to multiplexer 31. Based on a result of determination by the determining means, only EDID of one of the EDID storage memories is outputted.

A rough block diagram showing the constructions around the storage means in the present invention and Goddard et al. is attached hereto. The outstanding difference will be clear from a comparison between these constructions.

Fig. A Goddard et al.

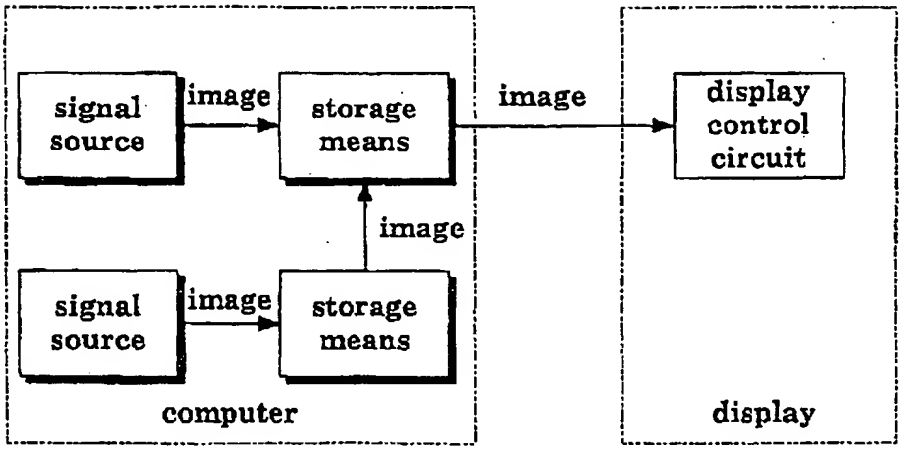

Fig. B Present Invention